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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,141	04/01/2004	Heung-Lyul Cho	0630-1979P	6546
2292 7590 10/01/2009 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				
EXAMINER				
SCHECHTER, ANDREW M				
ART UNIT		PAPER NUMBER		
2871				
NOTIFICATION DATE		DELIVERY MODE		
10/01/2009		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary

Application No.

10/814,141

Applicant(s)

CHO ET AL.

Examiner

ANDREW SCHECHTER

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2009.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 15 and 24 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1, 15 and 24 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 01 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB-08)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3 September 2009 has been entered.

Response to Arguments

2. Applicant's arguments filed 3 September 2009 have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 1 is objected to because of the following informalities: "phtoresist" in line 28 should be "photoresist". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 24 recites "sequentially forming a gate insulating layer, a semiconductor layer, a high-concentrated N+ layer and a conductive layer over the substrate including the gate line", as amended on 11 March 2009. It then recites using an active photoresist pattern to sequentially remove the high-concentrated N+ layer and the semiconductor layer" without mentioning the conductive layer. As amended on 3 September 2009, it then recites "forming a conductive layer over the substrate including the high-concentrated N+ layer and the semiconductor layer" and recites removing it using another photoresist layer patterned by lithography. Thus, the conductive layer used to create the source and drain electrodes is recited as being formed twice. The claim language is therefore unclear as to the method being claimed, so claim 24 is rejected as unclear.

The confusion appears to have arisen due to claim 24 being amended on 11 March 2009 to refer to the (withdrawn species) embodiment of Fig. 5, and then being amended on 3 September 2009 to refer to the (elected species) embodiment of Fig. 3. The present claim language contains elements of each species. Since the intent of the applicant [see p. 6 of their Remarks] was to direct claim 24 to the elected invention, it is assumed for examining purposes that the limitations relating to Fig. 5 were meant to have been removed, specifically at least removing "and a conductive layer" in line 13.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 15, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Deane et al.*, U.S. Patent No. 6,686,229 in view of official notice / admitted prior art, in view of *Chae* US 2002/0135710, and further in view of *Okazaki et al.*, U.S. Patent No. 5,127,330.

Deane discloses [see Fig. 1, for instance] a fabrication method of a liquid crystal display device, comprising: providing a substrate [1], forming a gate line [5] on a substrate by applying a gate photoresist pattern by a first printing process [col. 7, lines 60-67], removing the gate photoresist pattern [an inherent or implicitly-understood part of the process]; sequentially forming a gate insulating layer [13], a semiconductor layer [17], and a high-concentrated N⁺ layer [19] over the substrate and the gate line; forming an active photoresist pattern on the high-concentrated N⁺ layer by a second printing process [col. 7, lines 60-67]; forming an active region including the high-concentrated N⁺ layer by applying an active photoresist pattern by the second printing process [col. 7, lines 60-67], wherein the active region is formed by sequentially removing the high-concentrated N⁺ layer and the semiconductor layer using the active photoresist pattern formed by the second printing process as a mask [see Fig. 1b]; removing the active resist pattern [an inherent or implicitly-understood part of the process]; forming a

conductive layer [23] over the active region and the gate insulating layer; forming a source/drain electrode [29, 27]; forming a passivation layer [33] over the substrate and the source and drain electrodes; forming a contact hole photoresist pattern over the passivation layer by a third printing process [col. 6, lines 17-22]; removing the passivation layer by using the contact hole photoresist pattern as a mask to form a contact hole [35]; removing the contact hole photoresist pattern [an inherent or implicitly-understood part of the process]; forming a pixel electrode layer over the passivation layer and the contact hole; forming a pixel electrode photoresist pattern by a fourth printing process [col. 7, lines 60-67], and removing the pixel electrode layer by using the pixel electrode photoresist pattern as a mask to form a pixel electrode [37].

For the steps of forming the gate line, forming the semiconductor layer and N⁺ layer, and forming the pixel electrode, the reference describes directly printing the layers onto the substrate [as can be seen from the "tails" shown in the figures, for instance]. However, the reference also explicitly states [col. 7, lines 60-67] that these printing processes can be replaced with the process of covering the substrate with the material of the layer, printing a photoresist pattern onto the material, and etching to pattern the layer. The reference also provides motivation to do so, in that it avoids the need to use conventional photolithography to process the photoresists, thus lowering costs while not needing to directly print the layer. The examiner has therefore treated the relevant claim limitations as explicitly disclosed by the reference, as noted above; alternatively, they could be considered as not disclosed by the particular embodiment of Fig. 1 (and initial discussion thereof), but obvious to one of ordinary skill in the art at the

time of the invention due to these teachings of *Deane* [col. 7, lines 60-67]. In either case, these claim limitations are met by *Deane*.

Deane does not explicitly disclose depositing a photoresist layer over the conductive layer, applying a mask over the photoresist layer, and performing a lithography process, to thereby form the source and drain electrodes. Instead, *Deane* merely states that the conductive layer is "then patterned using conventional photolithography" [col. 5, lines 35-36]. The examiner took official notice that it was well-known in the art for conventional photolithography to include steps of depositing a photoresist layer over a conductive layer, applying a mask over the photoresist layer, and performing a lithography process to form a photoresist layer pattern [this taking of official notice was not traversed by the applicant, therefore the statement is considered admitted prior art, see MPEP 2144.04]. It would have been obvious to one of ordinary skill in the art at the time of the invention to have these steps in the method of *Deane*, motivated by the desire to use conventional photolithographic techniques, having high reliability and precision, to form the source and drain electrodes.

Deane does not disclose sequentially removing the conductive layer and the high-concentrated layer above the channel region by using the photoresist layer pattern as a mask to form a source and drain electrodes. Instead, the photoresist layer pattern is used as a mask to remove the conductive layer to form a source and drain electrodes and the photoresist layer pattern is then removed; the source and drain electrodes themselves (instead of the identically shaped photoresist layer pattern) are then used as the mask to remove the high-concentrated layer above the channel region.

Chae discloses [see Fig. 6C, paragraph 0061, for instance] a method of forming an analogous TFT, in which the source and drain electrodes [35, 37] are formed, the photoresist is removed, and the source and drain electrodes are then used as the mask to remove the high-concentrated layer [47], just as in *Deane*. *Chae* then goes on to say [paragraph 0062] that alternatively the photoresist can be left in place and used as the mask in removing the high-concentrated layer, just as in the present application. This is evidence that the two sequences are considered art-recognized equivalents. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the photoresist as the mask for removing the high-concentrated layer, motivated by the art-recognized equivalence of the two methods. (Also, as above, removing this photoresist layer pattern after it has served its purpose is an inherent or implicitly-understood part of the process.)

Regarding the additional limitations that the first to fourth printing processes are roller printing processes, the examiner previously took official notice that roller printing was known in the art, and as this was not traversed by the applicant, this was taken as admitted prior art [see MPEP 2144.04]; the use of roller printing was held to have been obvious to one of ordinary skill in the art at the time of the invention in this case in *Deane*, motivated by its being a reliable, cost-effective technique for printing. This remains valid. However, the taking of official notice did not extend to the newly recited details of the roller process, namely that each of the first to fourth roller printing processes include: providing a cliché having an intaglio pattern of a groove form; depositing a predetermined amount of photoresist on the cliché; rotating a roller on the

cliché to transfer the photoresist contained in the cliché onto a surface of the roller; and rotating the roller on the substrate to re-transfer the photoresist contained in the roller onto the substrate thereby forming a photoresist pattern on the substrate.

Okazaki et al. discloses [see Figs. 8-9, for instance, and discussion thereof] an analogous method in which roller printing is used to pattern a resist onto a surface in order to etch a layer [7]. The process includes providing a cliché [1] having an intaglio pattern of a groove form; depositing a predetermined amount of photoresist [3] on the cliché; rotating a roller [9] on the cliché to transfer the photoresist contained in the cliché onto a surface of the roller [Fig. 8b]; and rotating the roller on the substrate to re-transfer the photoresist contained in the roller onto the substrate [Fig. 8c] thereby forming a photoresist pattern on the substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a roller printing process in the above device, motivated by it being a conventional roller printing technique which is well-understood and would not require unnecessary experimentation, for instance.

Claim 1 is therefore unpatentable.

Since the other steps are done by printing rather than conventional photolithography, the mask applied over the photoresist layer in the step of applying the mask is the only mask applied throughout the method of the independent claim, so claim 15 is also unpatentable.

Considering claim 24, modified as discussed above under 35 USC 112, 2nd paragraph, the method discussed above meets all its recited limitations, so claim 24 is also unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/
Primary Examiner, Art Unit 2871
Technology Center 2800
26 September 2009